REMARKS

Claims 1-17 are pending in the application, with claims 1, 6 and 11 being the independent claims. Based on the following remarks, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

Rejections under 35 U.S.C. § 103(a)

Claims 1, 4-6, 9 and 10 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,370,675 (hereinafter referred to as "Matsumura") in view of U.S. Patent No. 6,704,895 (hereinafter referred to as "Swoboda"). Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Matsumura in view of Swoboda and further in view of U.S. Patent No. 5,931,962 (hereinafter referred to as "Dang"). Claims 11-13 and 16 and 17 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Matsumura in view of Swoboda and further in view of U.S. Patent No. 5,872,952 (hereinafter referred to as "Tuan") and U.S. Patent No. 6,550,036 (hereinafter referred to as "Panis"). Claims 14 and 15 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Matsumura in view of Swoboda and further in view of Tuan, Panis and Dang. Applicants respectfully traverse these rejections since Matsumura, Swoboda, Dang, Tuan and/or Panis, either taken alone or in combination, do not teach or suggest each element of independent claims 1, 6 and 11 for at least the following reasons.

Independent claims 1, 6 and 11 were previously amended to each include two different types of determinations. The first determination includes determining, in the virtual test

environment, an indication of a signal transmission time of the actual electronic device in the actual test environment. The second determination includes determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. Both of these two different types of determinations are then used in independent claims 1, 6 and 11 to evaluate the integrity of the input test signal and a resulting output signal from the virtual device.

The Examiner acknowledges that Matsumura does not expressly teach either of these two types of claimed determinations. The Examiner points to the same text in Swoboda (CL6, L26-31; CL12, L45-57; CL44, L10-19) to show both of these different types of determinations. Although Applicants respectfully disagree with the Examiner that the cited text in Swoboda teaches or suggests either of these types of determinations, Applicants would like to point out that the same cited text in Swoboda certainly does not teach or suggest both different types of claimed determinations.

The Examiner states that the cited text in Swoboda would allow for simulating the operation of the target chip and key peripheral features including timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). Applicants respectfully disagree with the examiner that these possible benefits of the cited text in Swoboda teaches or suggests performing the claimed two different types of

determinations in independent claims 1, 6 and 11. Accordingly, for at least this reason, independent claims 1, 6 and 11 (and their dependent claims 2-5, 7-10 and 12-17) are patentable over Matsumura, Swoboda, Dang, Tuan and/or Panis, either taken alone or in combination. Accordingly, Applicants request that the rejections under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

INVITATION FOR A TELEPHONE INTERVIEW

The Examiner is invited to call the undersigned, Molly A. McCall, at (703) 633-3311 if there remains any issue with allowance of the case.

CONCLUSION

Applicants respectfully submit that all of the stated grounds of rejection have been properly traversed accommodated or rendered moot. Applicants believe that a full and complete response has been made to the outstanding Office Action. Thus, Applicants believe that the present application is in condition for allowance, and as such, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections, and allowance of this application.

Respectfully submitted,

Intel Corporation

Dated: ___2-28-05____

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P10752 Reply to Final OA

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

2-28-05
Date of Deposit

Katherine C. Jennings
Name of Person Mailing Correspondence

Katherine C. Jennings 2-28-05
Signature Date